



Fig. 1

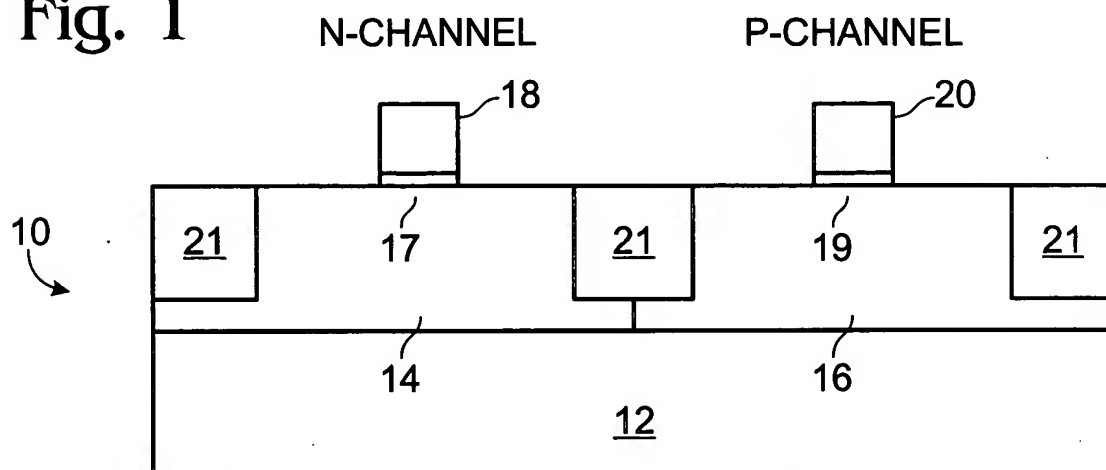


Fig. 2

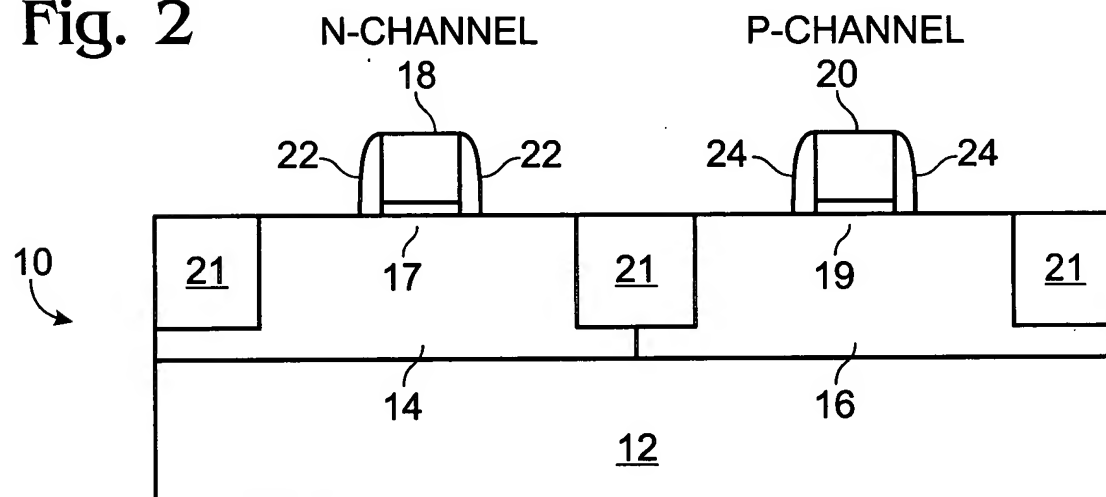
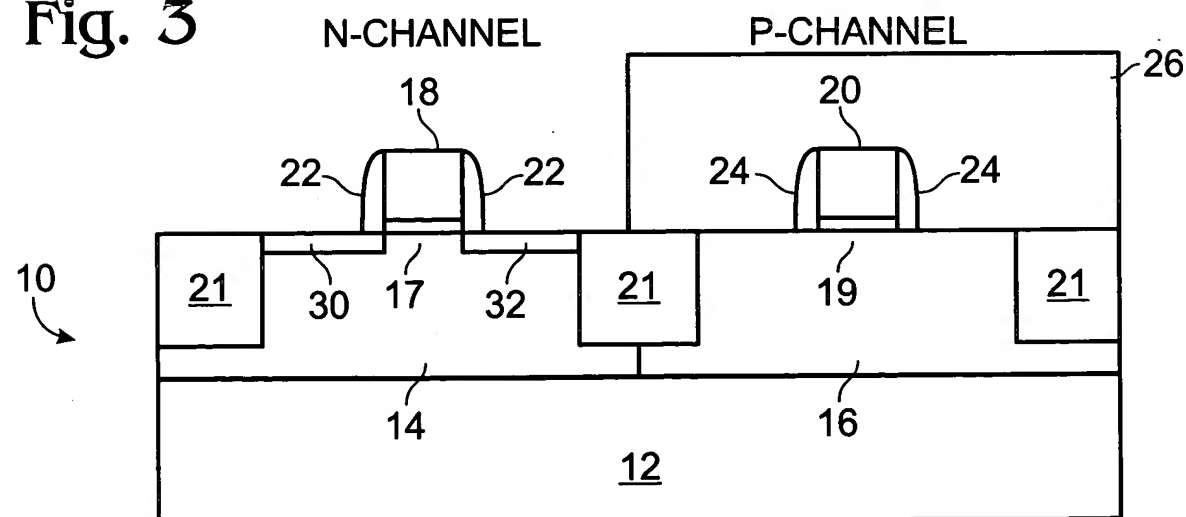
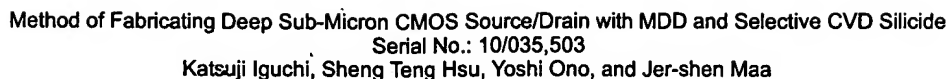


Fig. 3





A cross-sectional view of a semiconductor device 10. The device features a substrate 12 with a top surface 14. On the left, an N-channel region 16 is formed, containing a gate stack 18 and a channel region 17. The gate stack 18 includes a gate dielectric 22 and a gate electrode 42. The channel region 17 is defined by a gate electrode 42. The N-channel region 16 is separated from the P-channel region 20 by a channel stop 30. The P-channel region 20 contains a gate stack 24 and a channel region 19. The gate stack 24 includes a gate dielectric 44 and a gate electrode 44. The channel region 19 is defined by a gate electrode 44. The P-channel region 20 is separated from the N-channel region 16 by a channel stop 38. The device is surrounded by a passivation layer 21. The N-channel region 16 is labeled "N-CHANNEL" and the P-channel region 20 is labeled "P-CHANNEL".



Fig. 7

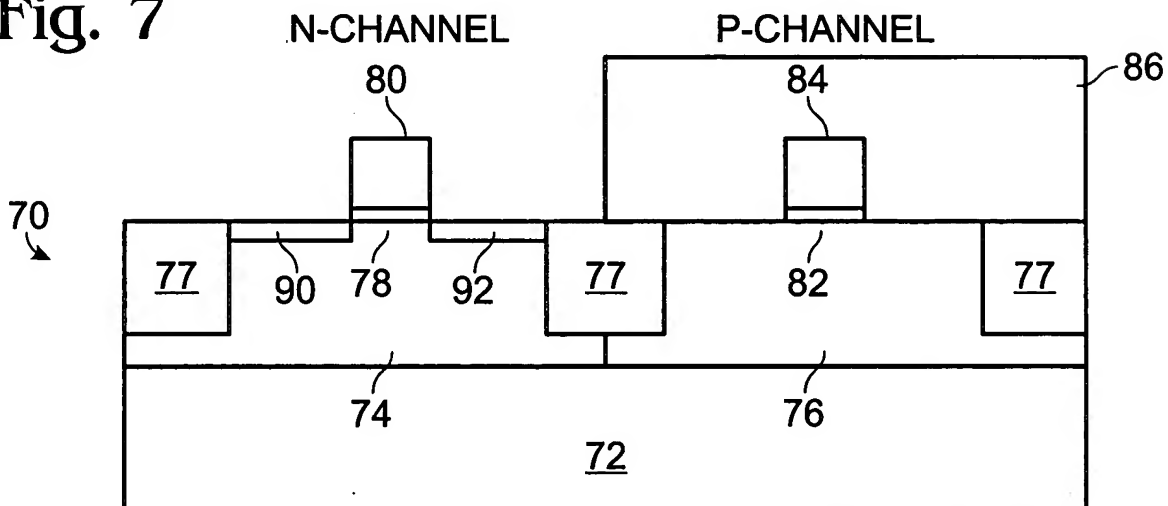


Fig. 8

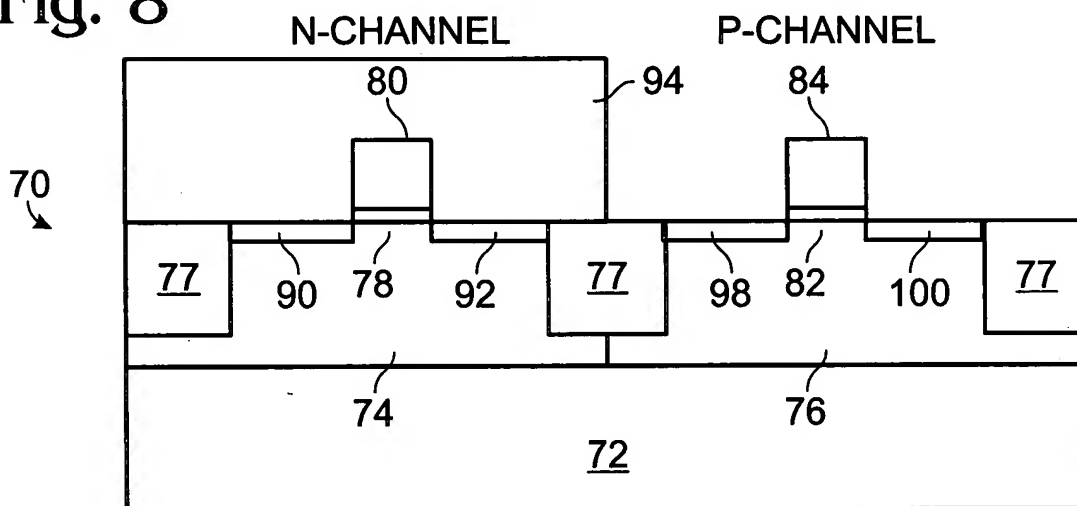


Fig. 9

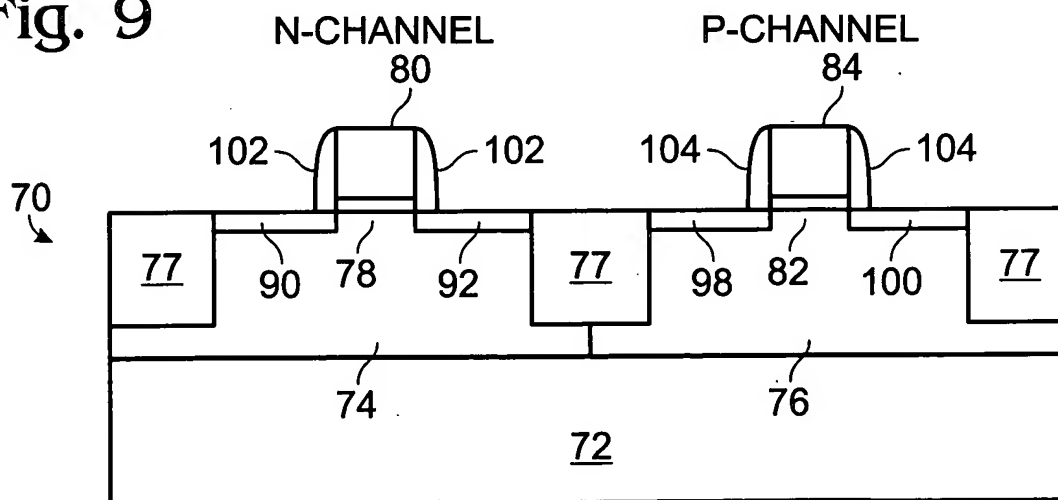




Fig. 10

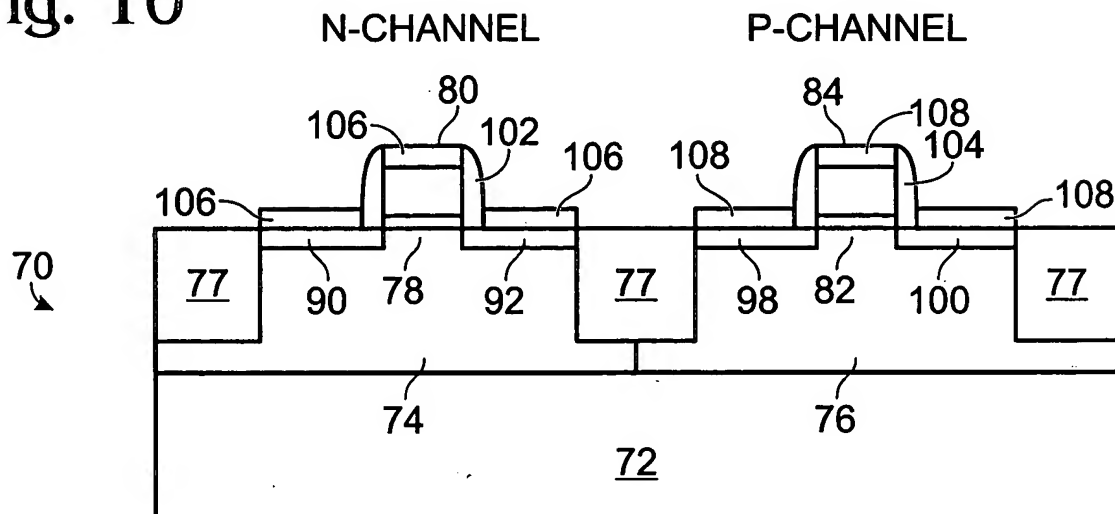


Fig. 11

